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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/018,783	02/04/1998	THOMAS L. RITZDORF	11928US01	1242

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PERKINS COIE LLP
P.O. BOX 1247
PATENT-SEA
SEATTLE, WA 98111-1247

EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/018,783	RITZDORF ET AL.
	Examiner	Art Unit
	Ori Nadav	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2005*.

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6,8-11,13-17 and 24-95* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6,8-11,13-17 and 24-95* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/05/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

Claims 1, 3, 4, 6, 8-11, 13-17 and 24-95 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitation of annealing process at a temperature below certain temperature, as recited in claims 1, 6, 10, 11, 24, 30, 51, 57, 70, 83, is held to be indefinite since applicant does not recite a lower limit to the temperature.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claims 1, 3, 4, 6, 8-11, 13-17 and 24-95, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Venkatraman (5,677,244) in view of Dubin et al. (5,972,192).

Regarding claim 10, Venkatraman teaches in figure 2 and related text a method for filling recessed microstructures at a surface of a semiconductor work-piece, the work-piece including at least one dielectric layer 15, with copper metal 14, 41 comprising:

depositing copper 14, 41 into the recessed micro-structures using an electrochemical process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures; and

subjecting the surface of the semiconductor work-piece with the deposited copper to an elevated temperature annealing process at a temperature selected to be below a predetermined temperature at which the dielectric layer would suffer substantial degradation.

Venkatraman does not state that the dielectric layer is a low-K dielectric layer.

Dubin et al. teach a low-K dielectric layer (column 2, line 31).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a low-K dielectric layer in Venkatraman's device in order to improve the characteristics and the insulation of the device.

Regarding claims 11, 17, 29, 50 and 52, Venkatraman teaches in figure 2 and related text a method for filling recessed microstructures at a surface of a semiconductor work-piece with copper metal comprising:

providing a semiconductor work-piece with a feature that is to be connected with copper metallization;

applying at least one dielectric layer over a surface of the semiconductor work-piece including the feature;

providing recessed microstructures in the at least one dielectric layer;

preparing a surface of the work-piece including the recessed microstructures with a metal seed layer 13 for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer 14, 41 onto the surface of the work-piece using a process that generates copper grains that are sufficiently small to substantially fill the recessed microstructures;

annealing the electrochemically deposited copper for a predetermined period of time at an elevated temperature selected to be below a predetermined temperature at which the dielectric layer would substantially degrade; and

removing copper metallization from the surface of the work-piece except from the recessed microstructures after the annealing of the copper using CMP (see figure 1).

Venkatraman does not state that the dielectric layer is a low-K dielectric layer.

Dubin et al. teach a low-K dielectric layer (column 2, line 31).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a low-K dielectric layer in Venkatraman's device in order to improve the characteristics and the insulation of the device.

Regarding claims 3-4, 8-9, 24, 30, 51, 53, 57, 70 and 83, Venkatraman teaches in figure 2 and related text substantially the entire claimed structure, as applied to claim 11 above, except depositing the copper layer using an electrolytic process.

Dubin et al. teach depositing the copper layer using an electrolytic process.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to deposit the copper layer in Venkatraman's device using an electrolytic process, in order to simplify the processing steps of making the device by using conventional deposition method.

Regarding claims 24, 35-36, 57, 70 and 83, Venkatraman teaches in figure 2 and related text subjecting the surface of the semiconductor work-piece with the deposited copper to an elevated temperature annealing process at a temperature below about 250 to 300 degrees Celsius for a time period that is sufficient to increase the grain size of the deposited copper (column 4, lines 13-14).

Regarding claims 1, 32, 37-38, 51, 58-59, 71-72 and 86-87,Venkatraman teaches in figure 2 and related text substantially the entire claimed structure, as applied to claim 11 above, except subjecting the copper to a temperature annealing process at a temperature below about 100 degrees Celsius.
Venkatraman teaches in figure 2 and related text subjecting the surface of the semiconductor work-piece with the deposited copper to an elevated temperature annealing process at a temperature about 150 to 390 degrees, and that the anneal temperature can be varied to adjust the characteristics of the copper (column 4, lines 13-18).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to anneal the copper in Venkatraman's device at a temperature below about 100 degrees Celsius, in order to adjust the characteristics of the copper according to the requirements of the application at hand.

Regarding claims 42, 44-46, 64-67, 70, 78-80, 83-85 and 93, Venkatraman teaches in figure 2 and related text substantially the entire claimed structure, as applied to claim 11 above, except applying electroplating power to the seed layer as a first power level for a predetermined first period of time and then applying electroplating power to the seed layer a higher second power level, wherein the forward pulsed waveform is at a frequency of between 1 and 1000 Hz.

Dubin et al. teach applying electroplating power to the seed layer as a first power level for a predetermined first period of time and then applying electroplating power to the seed layer a higher second power level, wherein the forward pulsed waveform is at a frequency of between 1 and 1000 Hz (column 8, lines 6-61).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply electroplating power to the seed layer as a first power level for a predetermined first period of time and then apply electroplating power to the seed layer a higher second power level, wherein the forward pulsed waveform is at a frequency of between 1 and 1000 Hz, in Venkatraman's device, in order to improve the characteristics of the copper layer.

Regarding claim 1, Venkatraman teaches in figure 2 and related text substantially the entire claimed structure, as applied to claim 11 above, except stating that the copper is deposited using an electrochemical process.

Dubin et al. teach depositing copper using an electrochemical process (column 7, lines 1-6).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to deposit the copper in Venkatraman's device by using an electrochemical process, in order to simplify the processing steps of making the device by using conventional deposition method.

Regarding claims 33, 39-40, 51, 60-61, 73-74 and 88-89, Venkatraman teaches in figure 2 and related text substantially the entire claimed structure, as applied to claim 11 above, except an annealing process for less than 15 minutes and less than one minute.

Venkatraman teaches in figure 2 and related text that the anneal time vary to adjust the characteristics of the copper (column 4, lines 13-18).

Dubin et al. teach pulse time less than one minute.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an annealing process for less than 15 minutes and less than one minute in Venkatraman's device, in order to adjust the characteristics of the copper according to the requirements of the application at hand.

Regarding claims 13-16, 26-28, 55-56, 63, 76 and 91, Venkatraman teaches in figure 2 and related text applying a metal seed layer 30 over the barrier layer 13 using CVD and PVD.

Response to Arguments

Applicant's arguments with respect to claims 1, 3, 4, 6, 8-11, 13-17 and 24-95 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
2/17/06

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800